Ring Oscillator Frequency Stability Improvement Techniques for Crystal-Free Communication Systems

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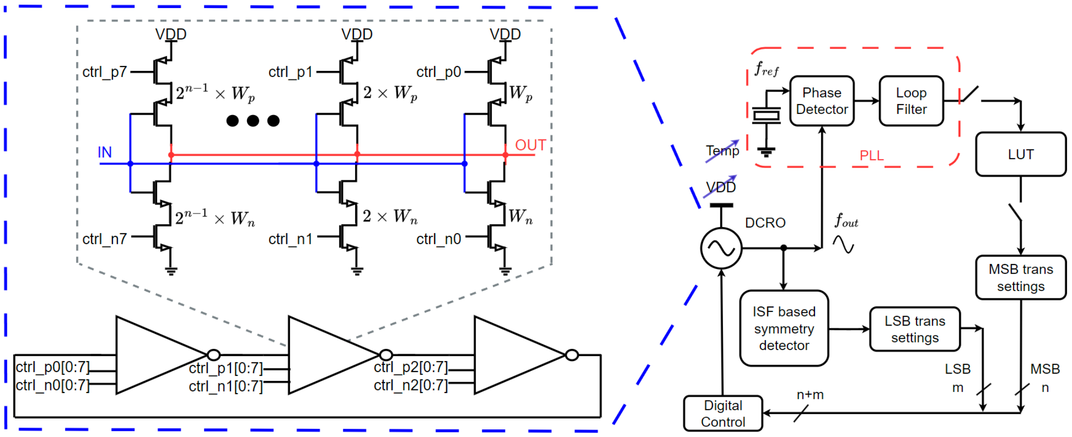

Figure 1: Digitally Controlled Ring Oscillator (DCRO) with binary-weighted transistors for carrier and symmetry tuning. Control words are generated via PLL-driven calibration and stored in LUTs for crystal-free real-time operation.

Abstract

This work aims to enable crystal-free communication through Ring Oscillators (ROs) by addressing their flicker noise sensitivity. We propose a Digitally Controlled Ring Oscillator (DCRO) using current-starved inverter delay cells with binary-weighted transistor DACs. These enable real-time digital control of inverter symmetry, reducing flicker noise upconversion without requiring many analog IOs. Larger DAC transistors control frequency and smaller ones control symmetry. The frequency control circuit may adopt a dual-mode architecture: a calibration mode using an external PLL to sweep across temperature and supply corners, as well as other possible factors, generating a multi-dimensional LUT of control words; and a free-running mode where the PLL is disabled and the DCRO is operated from on-chip LUT-based control. For waveform symmetry control, an ISF based symmetry detector can be used. Together, the DCRO and control techniques aim to deliver a low-power, inductor-free solution for crystal-free wireless communication. Machine learning methods may also be explored to generalize control and reduce calibration across dies.

CCS Concepts

• **Hardware → Radio frequency and wireless circuits**; **Clock generation and timing**; **Emerging architectures**;

Keywords

RF oscillators, phase noise, jitter, crystal-free IoT, frequency stability

1 Introduction

Crystal-free radios reduce power, area, and cost by eliminating the PLL and crystal, enabling low-cost IoT sensing with tiny motes. Without a crystal, LO phase noise degrades performance, causing issues like reciprocal mixing and drift [2]. LC-based crystal-free LOs [3] exist, but require large, non-scalable inductors. Ring Oscillators (ROs) require less area but suffer from poor phase noise, especially in crystal-free settings. While white noise in ROs can be mitigated by dissipating more power, reducing flicker noise upconversion, which results from waveform asymmetry, remains challenging [1]. Process mismatches lead to asymmetric inverter delays, increasing the $1/f^3$ flicker corner. The symmetry of the transistors can be controlled by using the current starved configuration shown in Fig. 2, wherein, the transistors M_{n1} and M_{p1} are used to control the rise and fall times. Thus the voltage *ctrl_ni* for the inverter stage *i* controls its rise time, and voltage *ctrl_pi* for the inverter stage *i* controls its fall time. However, using these analog signals limits the number of inverters that can be controlled individually. If making an RO with a high number of inverters, this can easily result in a high analog I/O count for the chip.

2 Proposed Oscillator Design

We propose implementing each inverter as a parallel combination of binary weighted current starved inverters, all driven by the same RF input signal *IN* and driving the same RF output signal *OUT*. However, instead of using only two analog control signals *ctrl_n* and *ctrl_p*, we propose using separate digital control signals on each of the inverters which fully enable or disable these inverters. Combined together, they essentially implement a single digitally controlled current starved inverter, as illustrated in Fig. 1, wherein, the two words *ctrl_ni* $< 0 : N >$ and *ctrl_pi* $< 0 : N >$ for each delay stage *i* now behave as the digital equivalents of the analog control signals *ctrl_ni* and *ctrl_pi*. The term binary weighted here

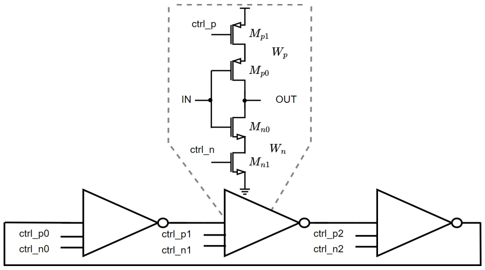

Figure 2: A current starved RO with analog control signals for rise and fall tuning.

refers to the transistor width scaling. The width of the smallest transistors is the minimum available in the technology, and the next ones are twice as wide and so on. Thus the effective width of the parallel combination of the transistors is controlled in real-time through the digital control word, similar to a DAC. Implementing each inverter through these binary weighted transistor DACs allows one to dynamically adjust the rise and fall characteristics of the individual delay stages through a simple digital control register, and we call this a Digitally Controlled Ring Oscillator (DCRO). This approach eases the IO requirements while still giving the designer the capability to control the symmetry of the oscillator in real-time, especially in processes with fixed transistor widths. The proposed circuit has been submitted for fabrication in Intel's 16 nm FinFET process and is expected to return for testing by the end of 2025.

There are two primary aspects of the oscillator's frequency that need to be controlled. Long term frequency drift and the short term frequency fluctuations or close-in phase noise. For the short term frequency fluctuations, the symmetry of the oscillator waveform needs to be maintained at all nodes. This can be accomplished by controlling the smaller transistors in the DAC, i.e., by adjusting the Least Significant Bits (LSBs) of the control words $ctrl\_ni < 0 : N >$ and $ctrl\_pi < 0 : N >$, through an ISF based symmetry detector circuit that measures the rise and fall durations and a control loop to ensure their symmetry, as shown in Fig. 3, and in Fig. 1.

For controlling the carrier drift, two different mechanisms can be considered. The first uses a charge-pump circuit to compare the DCRO's frequency with that received at the Rx antenna. As shown in Fig. 3, the Most Significant Bits (MSBs) are controlled by the charge-pump. However, the problem with this approach is that it lacks channel selectivity, as the charge-pump can potentially lock-on to any RF channel received at the antenna, which makes this method unfeasible for narrowband communication systems.

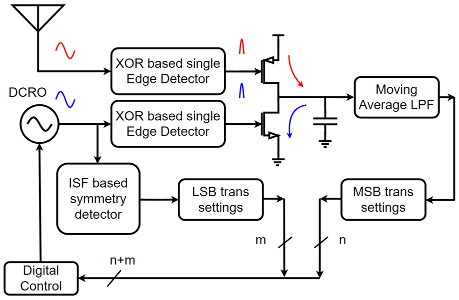

Figure 3: An oscillator control circuit with a charge-pump based control loop and an ISF based symmetry detector.

In another approach, the MSBs of the DCRO's digital control word are adjusted using a pre-computed Look Up Table (LUT). Consider the circuit shown in Fig. 1 that has an on-chip DCRO that is being controlled by a PLL and an off-chip crystal reference, similar to a traditional communication system. However, the PLL in the chip is specially designed so that it can be completely disabled, liberating the DCRO from the influence of the crystal reference and entering the free-running mode. Thus there are two primary modes of operation: one when the oscillator is being controlled by the PLL; the calibration mode, and one when it's running freely; the free-running mode. During the calibration mode, the crystal reference is replaced by a high fidelity bench-top frequency generator, and the frequency of this source is swept within the desired band of operation with the desired resolution. The MSBs of the digital control words that the PLL generates are then stored in a LUT. The entire calibration process is carried out in a temperature controlled environment, and the temperature and power supply voltage are swept as independent variables. Through this process, a multi-dimensional LUT is generated and stored on the chip, thus ending the calibration. Once the desired control words for different voltage and temperature conditions have been stored in the LUT, the system can then be used in the free-running mode, wherein, the external source is disconnected and the PLL is disabled. Instead, the on-chip circuit controls the MSB transistors using the data stored in the LUTs of the particular chip during calibration process to match the desired channel frequency. This approach is beneficial as the chip only needs to be calibrated once with the PLL and can operate in the free-running mode for real time operation with minimum power consumption.

3 Conclusion

This work presents a Digitally Controlled Ring Oscillator (DCRO) architecture for fully integrated, crystal-free wireless communication, eliminating off-chip references and inductors. Traditional ROs suffer from poor phase noise due to flicker noise upconversion caused by waveform asymmetry. The proposed DCRO uses current-starved inverter delay cells with binary-weighted transistor DACs, enabling real-time digital control of frequency and symmetry, improving phase noise without excessive analog IOs. Digital control is split between two circuits: LSBs adjust symmetry using an on-chip ISF-based detector, while MSBs set carrier frequency via two strategies: (1) a charge-pump loop locking to the received signal, and (2) a dual-mode system with initial PLL-based calibration and LUT-based free-running control. Together, these methods enable low-power, inductor-free, crystal-free communication.

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